(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 July 2003 (31.07.2003)

PCT

(10) International Publication Number
WO 03/063432 A1

(51) International Patent Classification⁷: H04L 12/64

(21) International Application Number: PCT/EP03/00203

(22) International Filing Date: 11 January 2003 (11.01.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02090038.7 25 January 2002 (25.01.2002) EP

(71) Applicant *(for all designated States except US)*: THOMSON LICENSING S.A. [FR/FR]; 46 Quai A. le Gallo, F-92100 Boulogne-Billancourt (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: HAUPT, Dieter [DE/DE]; Steinkuhler Garten 2, 31832 Springe (DE). GAEDKE, Klaus [DE/DE]; Schaumannweg 22, 30659 Hannover (DE). SCHWEIDLER, Siegfried [DE/DE]; Suedfeld 10, 30989 Gehrden (DE).

(74) Agent: SCHÄFERJOHANN, Volker; DEUTSCHE THOMSON-BRANDT GMBH, European Patent Operations, Karl-Wiechert-Allee 74, 30625 Hannover (DE).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,

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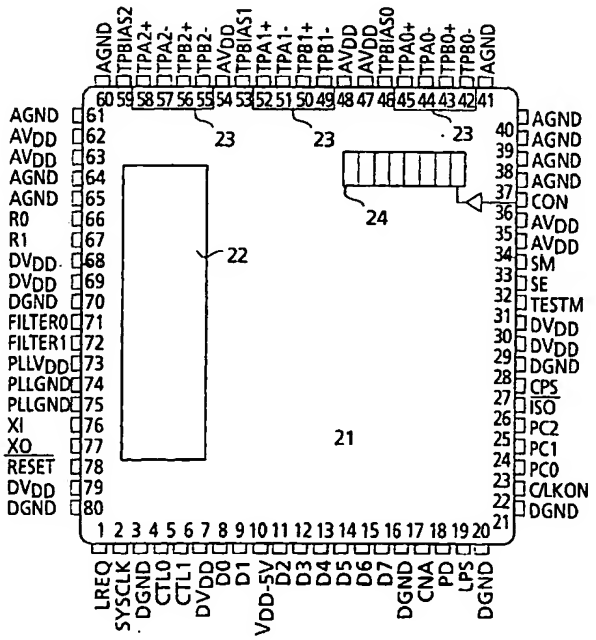
(54) Title: PHYSICAL LAYER CIRCUIT AND INTERFACE CIRCUIT



(57) Abstract: The invention deals with a physical layer circuit (21) for the IEEE1394 bus. Considered is a scenario where two clusters of 1394 devices are linked to each other by means of a wireless bridge (9). The devices of one cluster shall communicate with devices of the other cluster without being bridge aware. Under this scenario there are two different types of 1394 devices existing in each cluster. One device is a bridge portal and will have the bridge functionality. All the other 1394 devices in the cluster will not have the bridge functionality. As the device having the bridge functionality needs to have a specific buffer memory (22) for buffering node-ID packets, usually there are two different types of physical layer circuits required for the different types of 1394 devices. The invention deals with the problem of how it can be realized to use in both different types of 1394 devices the same type of physical layer circuit (21). The invention solves the problem by means of configuration means (24) in the physical layer circuit (21). These configuration means enable either to configure the physical layer circuit (21) as a bridge portal physical layer circuit supporting the bridge functionality by buffering said node-ID packets in said buffer memory (22) or else configuring the physical layer circuit (21) as a standard physical layer circuit that disables the buffering of said node-ID packets. The new type of physical layer circuit is pin compatible with a standard physical layer circuit.

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ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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